Design and Implementation of High Pumping Efficiency CMOS Charge Pump

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Abstract
In this paper, low threshold CMOS charge pump is designed and different analysis has been done. To remove the threshold drop as in Dynamic charge pump this architecture is used. This low threshold CMOS charge pump removes the threshold drop across the last diode connected transistor using a circuitry which provides dynamic switching.

Keywords
DC to DC Converter, Dynamic Charge Pump, Static Charge Pump, CTS Logic, Low Threshold, High Pumping

I. Introduction

A charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Charge pump circuits are capable of high efficiencies, sometimes as high as 90-95% while being electrically simple circuits.

Charge pumps use some form of switching device(s) to control the connection of voltages to the capacitor. For instance, to generate a higher voltage, the first stage involves the capacitor being connected across a voltage and charged up. In the second stage, the capacitor is disconnected from the original charging voltage and reconnected with its negative terminal to the original positive charging voltage. Because the capacitor retains the voltage across it (ignoring leakage effects) the positive terminal voltage is add to the original, effectively doubling the voltage. The pulsing nature of the higher voltage output is typically smooth by the use of an output capacitor.

Charge pumps can double voltages, triple voltages, halve voltages, invert voltages, fractionally multiply or scale voltages such as x3/2, x4/3, x2/3, etc. and generate arbitrary voltages, depending on the controller and circuit topology.

In 1976 J. F. Dickson designed a DC to DC converter using N MOS. This circuit is known as Dickson charge pump [1]. This charge pump is the basic architecture on which all other charge pump circuits are dependent. This circuit provides a higher output voltage from a lower input voltage, but due to threshold drop across the diode connected transistor in this architecture it is not useful in the low voltage applications. In 1998 J. Wu and K. Chang designed two new circuits which are useful in low voltage application. These two charge pumps are Static and Dynamic charge pump.

Static charge pump removes the threshold drop occurring in the Dickson charge pump, but it has a drawback of reverse charge sharing due to which the overall gain is decreased as compared with predicted gain. To remove this drawback J. Wu and K. Chang designs a new charge pump which uses Dynamic CTS (Charge transfer scheme) .In this scheme the N MOS switch is turned ON and Turned OFF dynamically as the CLK Phase changes. These circuits are useful in Low voltage applications. Dynamic charge pump have drawback of threshold drop across the last diode connected N MOS transistor. To remove this threshold drop a new architecture is proposed. This low threshold CMOS charge pump removes the threshold drop across the last diode connected transistor using a circuitry which provides dynamic switching.

The demand for low voltage application is today's industry need. The power savings that result from a decrease in the supply voltage has been one of the prime motivators for current research efforts, which focus on the development of circuit topologies that can operate with lower supplies. This low threshold CMOS charge pump has the advantage of providing a higher gain for lower supply voltages, so, it is useful in the applications where lower supply voltage is available and power saving is required.

II. Low Threshold CMOS Charge Pump

In Dynamic charge pump, there is a drawback of threshold drop at output node due to the diode connected transistors MD5.That transistor is used to avoid the fluctuations and reverse charge sharing at output node. To remove this threshold drop from the output, new charge pump architecture is designed. In this charge pump Two PMOS MP5, MP6 and one N MOS MN5 are used. The circuitry of this charge pump is shown in the figure 1. The functionality of the architecture is same as Dynamic charge pump till fourth pumping node. When Clk1 is low and Clk2 is high, due to charging of the capacitor, the voltage is increasing at node 4.Therefore due to inverter action PMOS become ON and all charge at node 4 passes to output. Now when clk 1 goes high and clk 2 goes low the C4 discharges and PMOS MP6 becomes off. Due to all this action this circuit provides dynamic switching at the output node.

III. Derivation Of Basic Working of a Charge Pump

The basic working of a charge pump can be explained using the circuit shown in fig. 2, in this circuit two diode connected MOS transistors M1 and M2, two capacitors C1 and C_{load} are used.C1 is connected to node B. Clk is connected to an inverter and through capacitor C1 it is connected to node B. In this circuit the value of clock is taken similar to VDD. In the given circuit initially the settling voltage at node B is

$$V_B=V_{DD}-V_t \quad (1)$$

At output

$$V_{load}=(V_{DD}-V_t)-V_t<V_B \quad (2)$$

When Clk is $=1(V_{DD})$,A=0 Capacitor charge by

$$Q=C_1(V_{DD}-V_t) \quad (3)$$

When clk goes from 1 to 0, A= V_{DD}, Then VB instantly goes up to

$$V_B=2V_{DD}-V_t$$

To remain potential difference across C1 constant the voltage at node B becomes

$$V_B=(2V_{DD}-V_t)-V_{DD}$$

$$V_B=V_{DD}-V_t$$

When the voltage at node B goes from $V_{DD}-V_t$ to $2V_{DD}-V_t$, as V_B becomes V_t above V_{laod}, M2 start conducting and Cload begin to charge. Again when Clk=1,V_A=0, M2 stops conducting, again the C1 charged to $V_{DD}-V_t$. After some consecutive Cycles

$$V_{load}=2(V_{DD}-V_t) \quad (4)$$

This shows that output voltage is increased corresponding to the input voltage. This is the basic concept used in all charge pump circuits.

In Dynamic charge pump voltage at output node is given by

$$V_{out} = V_{DD} + N\left[\left(\frac{C.V_{clk}}{C+C_s}\right) - \frac{I_0}{f\left(C+C_s\right)}\right] - V_{th} \quad (5)$$

Here N represents the total number of stages, for four stages N=4.

In low threshold CMOS charge pump, the threshold voltage drop occurring in equation 15 is eliminated. So, the output voltage of low threshold CMOS charge pump is given by

$$V_{out} = V_{DD} + N\left[\left(\frac{C.V_{clk}}{C+C_s}\right) - \frac{I_0}{f\left(C+C_s\right)}\right] \quad (6)$$

So, the low threshold CMOS charge pump provides a better gain then all other charge pumps.

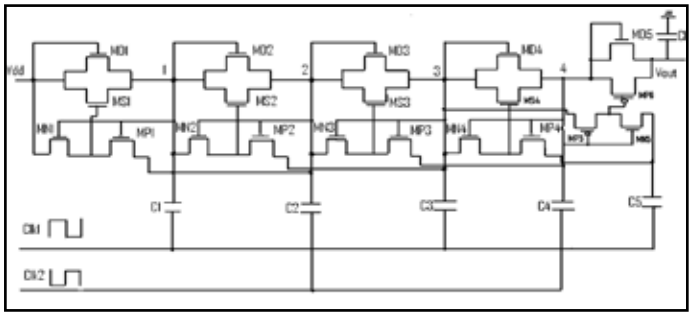


Fig. 1: Low Threshold CMOS Charge Pump

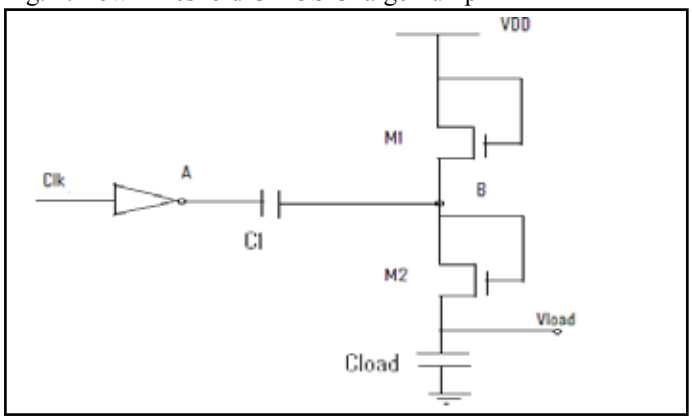


Fig. 2: Basic Single Stage for Charge Pump

IV. Schematic Design

A four stage schematic of low threshold CMOS charge pump is drawn in fig. 3, which consists of fourteen NMOS transistor, six PMOS transistor, five pumping capacitor, one load capacitor, two clock inputs and one DC input.

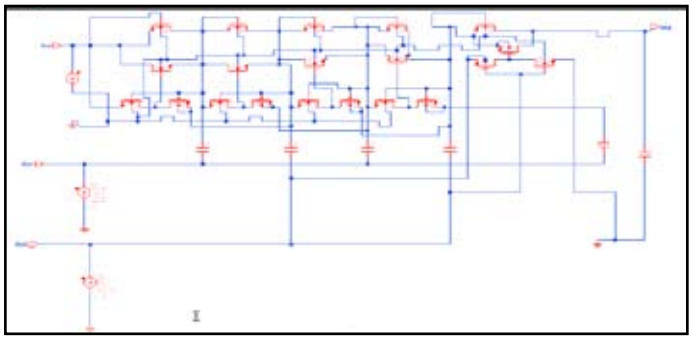
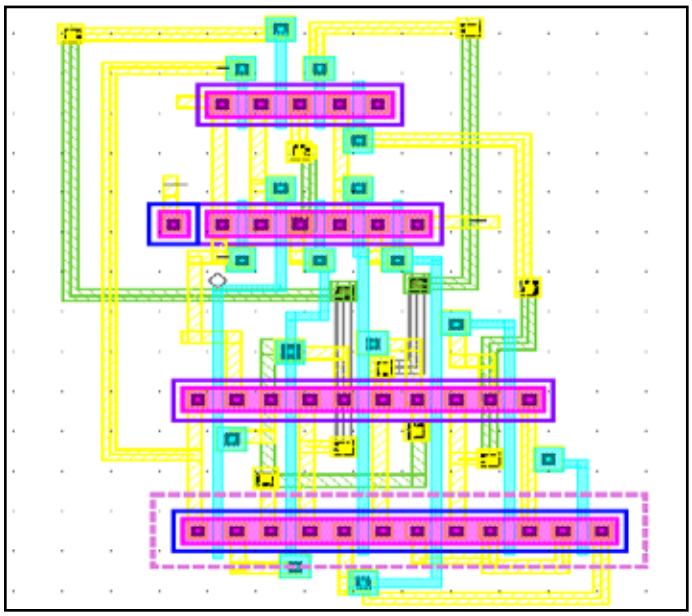


Fig. 3: Schematic of Low Threshold CMOS Charge Pump

V. Layout Design



VI. Simulation Results

Output voltage waveform is shown in fig. 4, in this waveform it is clear that output voltage is equal to 5.64 volts for an input of 1.8 volts.

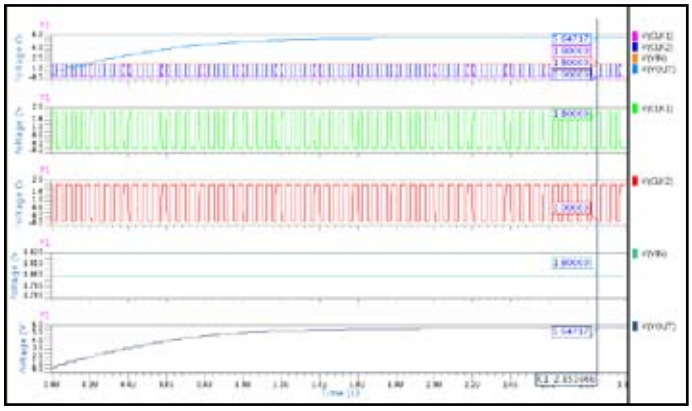
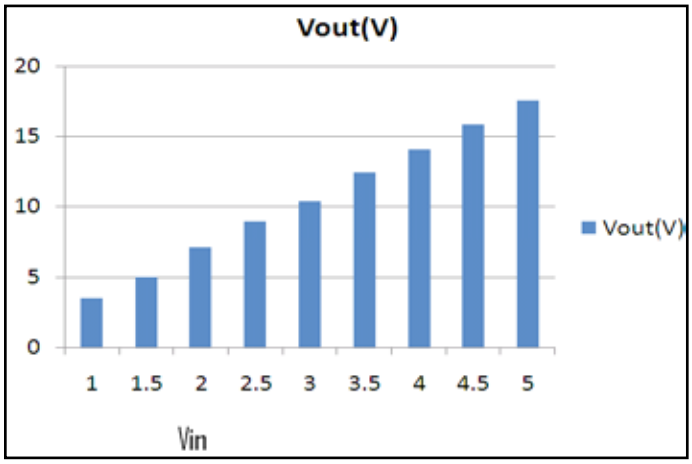


Fig. 4: Waveform of Four Stage Proposed Charge Pump

VII. Voltage Analysis

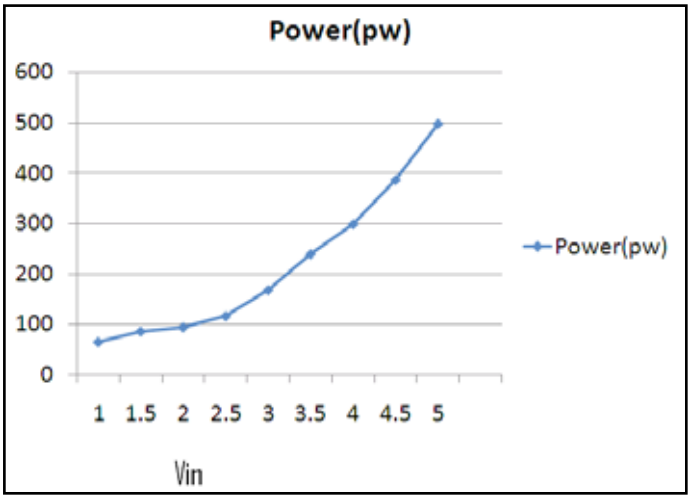
Graph 1shows the output voltage corresponding to different input voltages. It can be observed that output voltage increases as we increase our input voltage. This increase is due to the direct proportionality of output voltage to the input voltage



Graph 1 output Voltage vs. Different Input Voltages

VIII. Power Analysis

In this analysis output power corresponding to various input voltages is analyzed. In Graph 2 shows output power corresponding to different input voltages are shown.



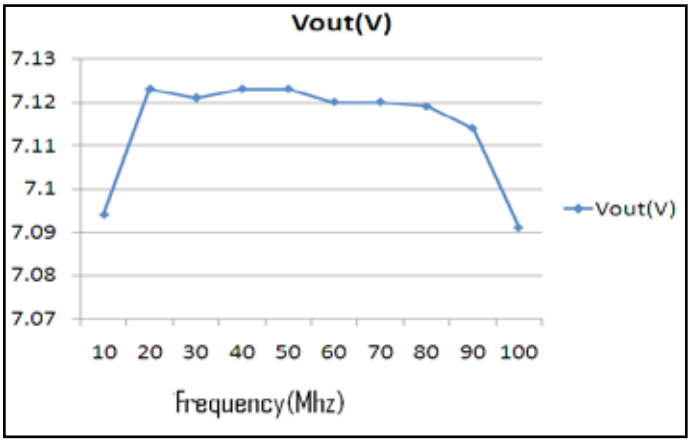
Graph 2 output power vs. different input voltages

This graph shows that as the input voltage increases the output power is also increases. It is known that output power is directly proportional to square of the input voltage, capacitance and frequency. Frequency and capacitance are kept constant, so power is proportional to square of supply input voltage theoretically, but some other parameter influences output power practically. So this type of behavior is observed.

IX. Frequency Analysis

Graph 3 shows output voltage of four stage Proposed charge pump for different frequencies. Here it is seen that for the frequency below 20 MHz and above 70 MHz gain is low. In the range 20 MHz to 70 MHz a constant gain is observed. This gain is due to the fact that at lower frequencies the pumping node are at higher voltage for a long time and the charge is leak through the MOS transistor.

At higher frequencies the gain becomes lower; this is due to the fact of fast charging and discharging of capacitors. At higher frequencies the capacitor cannot charge and the CLK phase changes due to this the gain decreases.

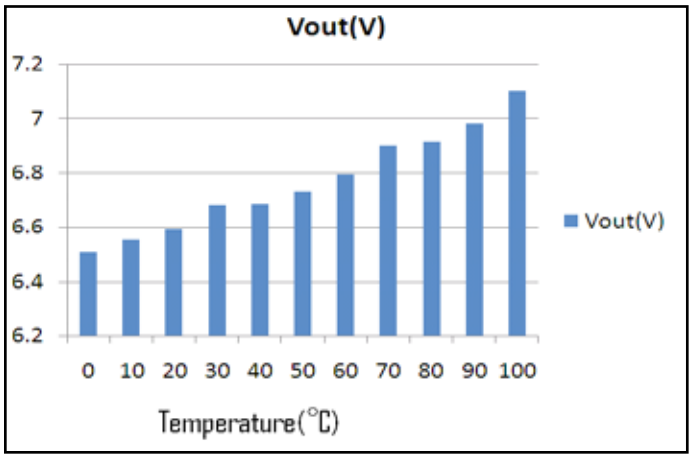


Graph 3 output voltage vs. different frequencies

X. Temperature Analysis

Graph 4 shows output voltage of low threshold CMOS charge pump for different Temperatures. Here, it is shown that the output voltage increases as the temperature increases. This phenomenon is observed because due to increase in temperature the conductivity of the channel in MOS transistor increases and more charges are transferred to capacitor and output voltage increases.

It can be observed that as the temperature increase the gain increases



Graph 4 output voltage vs. Different Temperatures

XI. Conclusion

A low threshold CMOS charge pump circuit, which uses both the N MOS switches and the PMOS switches to eliminate the body effect, has been designed. A novel CTS control scheme which combines the backward control scheme and the forward control scheme is proposed to obtain high voltage gain. In 180nm CMOS process, the simulation results have shown that much higher pumping efficiency can be achieved by the proposed charge pump compared with others.

References

[1] J. F. Dickson,"On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique", IEEE J. Solid- State Circuits, Vol. 11, pp. 374–378, June 1976.

[2] J. Wu, K. Chang,"MOS charge pumps for low-voltage operation," IEEE Journal of Solid-State Circuits, Vol. 33, pp. 592-597, Apr. 1998.

[3] Y. Tsukikawa, T. Kajimoto, Y. Okasaka, H. Miyamoto, H. Ozaki,"An efficient back- bias generator with hybrid pumping circuit for 1.5 v drams", VLSI Circuits, 1993. Digest of Technical Papers. 1993Symposiumon, pp. 85–86, May 1993.

[4] Y. S. Kikuzo Sawada, S. Masui,"An on-chip high-voltage generator circuit for eeproms with a power supply voltaige below 2v", Symposium on VLSI Circuits Digest of Technical Papers, 1995.

[5] K.-H. Choi, J.-M. Park, J.-K. Kim, T.-S. Jung, K.-D. Suh, "Floating-well charge pump circuits for sub-2.0v single power supply flash memories", VLSI Circuits, 1997. Digest of Technical Papers., 1997 Symposiumon, pp. 61–62, Jun1997.

[6] C.-F. Liang, S.-H. Chen, S.-I. Liu,"A digital calibration technique for charge pumps in phase-locked systems", Solid-State Circuits, IEEE Journal of, Vol. 43, No. 2, pp. 390–398, Feb. 2008.

[7] J.-S. Wang, C.-Y. Cheng, Y.-C. Liu, Y.-M. Wang,"A 0.67?w/mhz, 5ps jitter, 4 locking cycles, 65nm addll," Solid-State Circuits Conference, 2007. ASSCC '07. IEEE Asian, pp. 300–303, Nov. 2007.

[8] U.-K.M.G.C. T.Arun Rao,William McIntyre,"Noise-shaping techniquesapplied toswitched- capacitor voltage regulators", IEEE Journal of Solid-StateCircuits, 2005.
[9] G. Monna, J. Sandee, C. Verhoeven, E. Groenewold, A. Van Roermund,"Charge pump for optimal dynamic range filters", Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposiumon, Vol. 5, pp. 747–750, May-2 Jun 1994.
[10] J.-T. Wu, Y.-H. Chang, K. L. Chang,"1.2 v cmos switched-capacitor circuits", Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC, 1996 IEEE International, pp. 388–389, 479, Feb 1996.
[11] K.-H. Lee, Y.-J. Woo, H.-S. Han, K.-C. Lee, C.-S. Chae, G.-H. Cho,"Power-efficient series-charge parallel-discharge charge pump circuit for led drive", Power Electronics SpecialistsConference, 2008. PESC2008. IEEE, pp. 2645–2649, June 2008.
[12] D. Bingham,"Integrated dual charge pump power supply and rs-232 transmitter/receiver", U.S. Patent 4897774, 1990.
[13] F. Raab,"Average efficiency of class-g power amplifiers", Consumer Electronics, IEEE Transactions on, Vol. CE-32, No. 2, pp. 145–150, May 1986.
[14] Jaycar Electronics Reference Data Sheet: DCDCCONV.PDF (1)
[15] Y. Nakagome et al.,"An experimental 1.5-V 64 Mb DRAM", IEEE Journal of Solid-State Circuits, Vol. 26, pp. 465-472, April 1991.
[16] S. Singer,"Inductance-less up dc-dc convertor", IEEE Journal of Solid-State Circuits, Vol. SC-17, pp. 778-781, Aug. 1982.
[17] P. Gillingham et al.,"High-speed, high-reliability circuit design for megabit DRAM", IEEE Journal of Solid-State Circuits, Vol. 26, pp. 1171-1175, August 1991.
[18] W. Martino et al.,"An on-chip back-bias generator for MOS dynamic memory", IEEE Journal of Solid-State Circuits, Vol. SC-15, pp. 820-825, Oct. 1980.
[19] T. Byunghak, P. Gray,"A 10 b, 20 Msample/s, 35 mW pipeline A/D converter", IEEE Journal of Solid-State Circuits, Vol. 30, pp. 166-172, March 1995.

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