Design and Implementation of CTS CMOS Charge Pump

Sakshi Rajput
Maharaja Surajmal Institute of Technology, New Delhi, India

Abstract
This CMOS charge pump is suitable for low voltage applications, can be operate with very low voltage supply voltage. In this charge pump MOS transistor are used as charge transfer switches to eliminate the effect of threshold voltage in each pumping stage. The output of the dynamic inverter controllers the MOS switch of each pumping stage for reducing the risk of reverse current and for this we need not extra circuitry. The Charge pump circuit is able to generate booth positive and Negative voltage. The converter consists of a charge pump circuit operated at 20 MHz from 1.5V to 5V. The desired output voltages, 6.46V to 20V.

Keywords
Charge Pump, DC-DC Converter, Dickson Charge Pump, Dynamic Charge Pump, Static Charge Pump

I. Introduction

Charge pumps are used for driving analog switches in switched capacitor systems. It can be used in low-voltage mixed-mode circuits to supply power to certain analog parts, which requires relatively higher voltages for their operation. In battery-operated systems, low voltage CMOS design becomes essential for low power dissipation. As a result, the power supply voltages continue to scale down. However, certain parts of the system may require higher voltage for proper operation. Consequently, charge pump circuit is likely to become an important component in low power CMOS design. This thesis describes an existing charge pump circuit that improves the area efficiency of a conventional charge pump, and introduces a new charge pump circuit that further improves the area efficiency. This new charge pump circuit provides a very low output ripple with a smaller amount of capacitance than existing charge pumps, at the cost of a reduced output voltage and a small amount of additional power loss.

II. Design

The charge pump is a dc-dc converting circuit used to obtain a dc voltage higher or lower than the supply voltage or opposite in polarity to the supply voltage. Charge pump circuits use capacitors as energy storage devices. The capacitors are switched in such a way that the desired voltage conversion occurs. Charge pumps are useful in many different types of circuits, including low-voltage circuits, dynamic random access memory circuits, switched-capacitor circuits, EEPROM's and transceivers.
The goal of this research was to develop techniques to use less chip area to achieve the same output ripple as existing charge pump circuits. Power efficiency issues and design tradeoffs are also considerd.

A. Cockcroft-Walton Charge Pump

The first widely used voltage boosting circuit was the Cockcroft-Walton voltage multiplier. This circuit, shown in fig. 1, uses diodes and serially connected capacitors and can boost to several times the supply voltage. The Cockcroft-Walton charge pump provides efficient multiplication only if the coupling capacitors are much larger than the stray capacitance in the circuit, making it undesirable for use in integrated circuits.

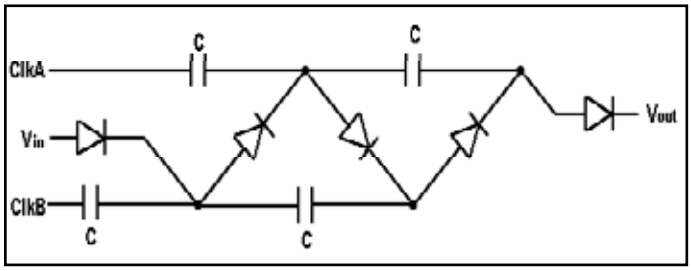


Fig. 1: 4-Stage Cockcroft-Walton Charge Pump

B. Dickson Charge Pump

In the Dickson charge pump circuit, the coupling capacitors are connected in parallel and must be able to withstand the full output voltage. This results in lower output impedance as the number of stages increases. Both circuits require the same number of diodes and capacitors and can be shown to be equivalent. The Dickson charge pump circuit shown in fig. 2, has been widely deployed for generating higher voltages. The diode-connected NMOS transistors are used instead of p-n junction diodes for implementing the circuit in standard CMOS process. The diode-connected NMOS allow the charge flow only in the direction of the output stage in ideal conditions. The charges are pushed from one stage to the next, resulting in higher DC voltage at the output.

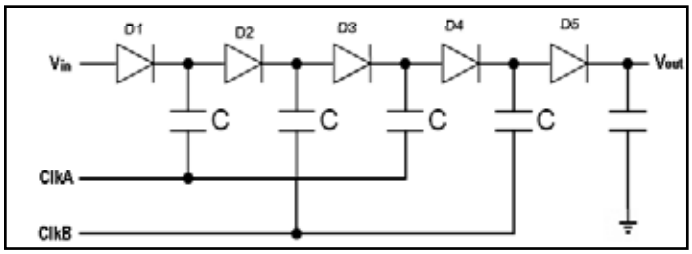


Fig. 2: 4-Stage Dickson Charge Pump

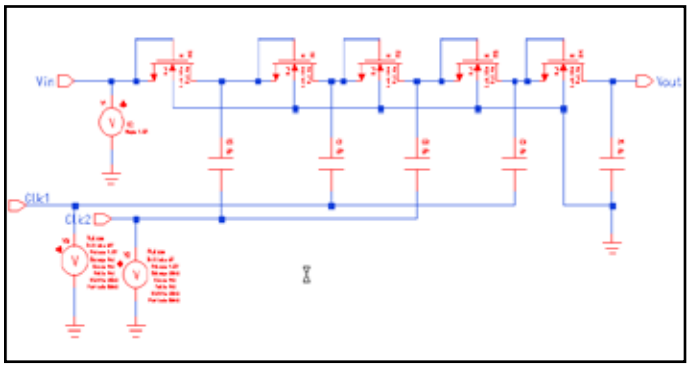


Fig. 3: 4-Stage Schematic of Dickson Charge Pump

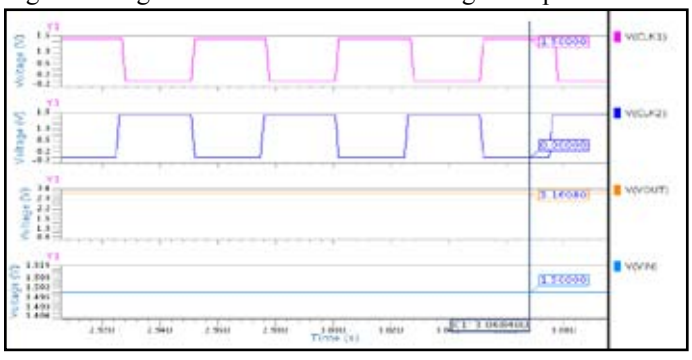


Fig. 4: Output Waveform of 4-Stage Dickson Charge Pump

The drawback of the Dickson charge pump circuit is that the boosting ratio is 3 degraded by the threshold drops across the diodes. The body effect makes this problem even worse at higher voltages.

C. Static Charge Pump

It uses charge transfer switches in addition to the diode-connected transistors to eliminate the threshold drop.

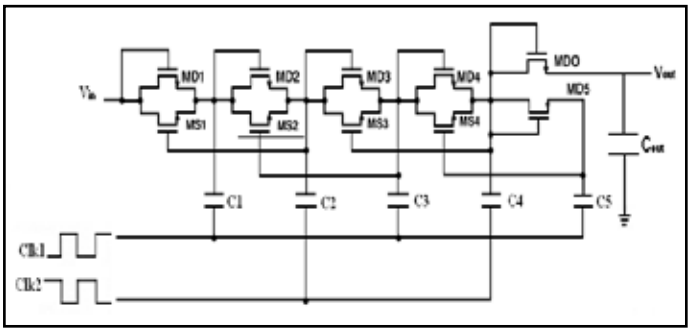


Fig. 5: 4-Stage Static Charge Pump

Static CTS charge pumps are new charge pumps employing dynamic switches to increase the voltage pumping gain. The basic idea behind these multipliers is to use MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode connected transistors which inevitably introduce a forward voltage drop at each node.

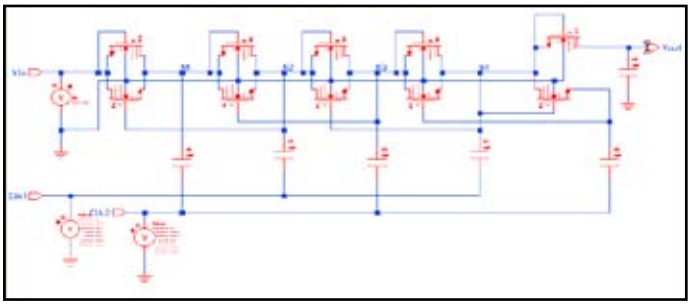


Fig. 6: 4-Stage Schematic of Static Charge

Compared with the Dickson charge pump, the Static Charge pump has a much better charge pumping performance.

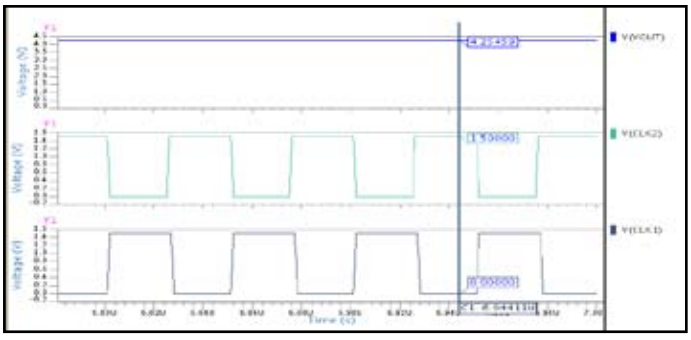


Fig. 7: Output Waveform of 4-Stage Static Charge Pump

But, there is one minor problem with this circuit configuration, namely, charge leakage in the reverse direction. When clock Clk1 is low, the voltage at nodes 2 and 3 is equal and 2.ΔV above the voltage at node 1. This reverse charge leakage phenomenon can be eliminated by adding pass transistors (both NMOS and PMOS) to the Static charge pump circuit. The function of these transistors is to apply dynamic control to the CTS's in order to turn them off completely when required and still be able to turn them on easily by the backward control voltage as in the Static charge pump case.

D. Dynamic Charge Pump

An improved design, which eliminates the previous problem by adding pass transistors to the previous circuit, this charge pump was designed for use in low-voltage circuits and is shown in fig. 7. Charge pump voltage boosters are also used in transceivers.

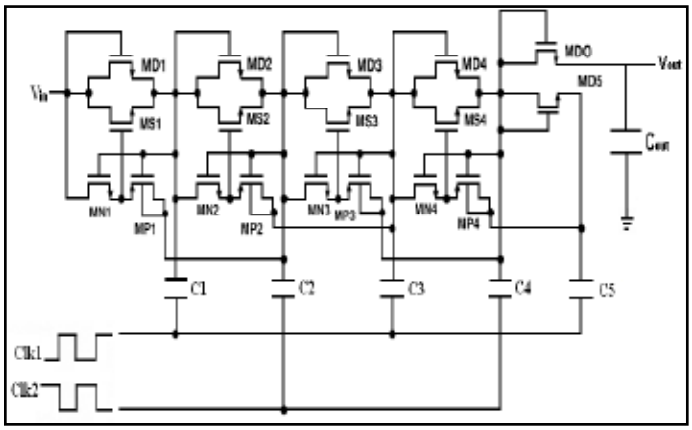


Fig. 8: 4-Stage Dynamic Charge Pump

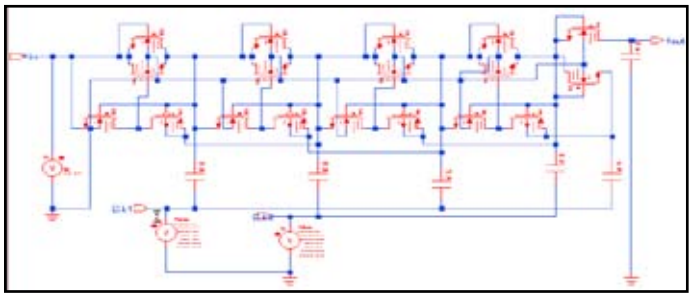


Fig. 9: 4-Stage Schematic of Dynamic Charge Pump

This circuit employs dynamic Charge Transfer Switches (CTS). Each of the CTS (MS's transistors) is controlled by the pass transistors MN's and MP's. The dynamic CTS are used to transfer charges from one stage to the next without suffering the problem of Vth voltage drop. The CTS's can be turned off completely when required and can also be turned on effectively by the higher voltage generated in the next stage. Thus, reverse charge flow is avoided, leading to increased efficiency. The output voltage of a 4-stage Dynamic charge pump is expected to be 5 x VDD in ideal conditions.

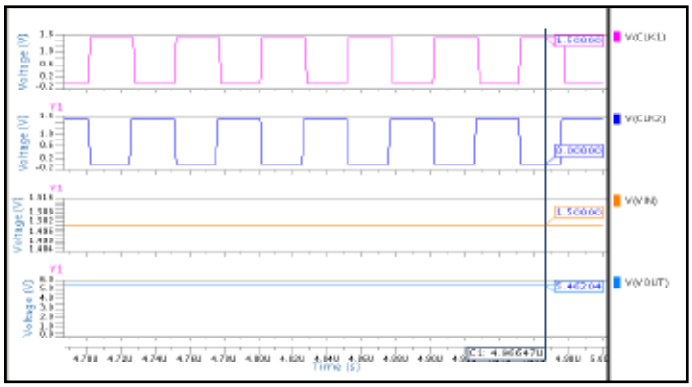


Fig. 10: Output Waveform of 4-Stage Static Charge Pump

E. High Efficiency CMOS Charge Pump for Low Voltage Operation

A charge pump circuit with a novel CTS (charge transfer switch) control scheme is to achieve better pumping efficiency in low voltage operation. The novel CTS control scheme employs the backward control of the NMOS CTS and the forward control of the PMOS CTS. The NMOS CTS has no substrate current during the dynamic control process and the PMOS CTS is able to eliminate the body effect of the output stage effectively. Hence, high pumping efficiency and high reliability can be achieved with this charge pump circuit.

The novel CTS control scheme is developed to enhance the pumping efficiency by controlling the NMOS CTS with the backward control scheme and controlling the PMOS CTS with the forward control scheme. The principle of the backward control scheme is to derive high voltage to control the NMOS switch from the following stage, and the principle of the forward control scheme is to derive low voltage to control the PMOS switch from the preceding stage.

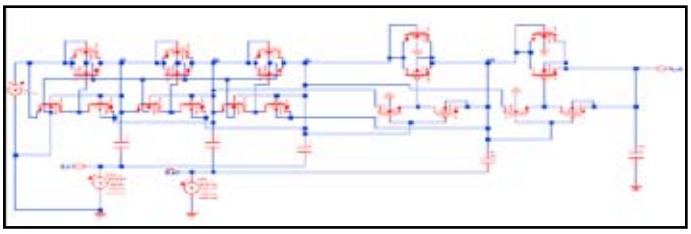


Fig. 11: 4-Stage Schematic of High Efficiency CMOS Charge Pump

F. Proposed Charge Pump

A MOS switch when is completely on can pass charge from its drain to its source similar to a forward biased diode. It has the advantage that almost no voltage drop occurs between its drain and source terminal. Replace the diode connected nMOS transistors of a classical Dickson charge pump with pMOS switches. If these switches are turned on and off at proper clock phases, they can allow the charge to be pushed in only one direction. In order to control the on/off operation of each switch, a dynamic inverter is inserted in each stage. The inverter works dynamically because its low and high voltages change during different clock phases and are different from the low and high voltages of the inverters of the other stages. The control voltage of each inverter is derived from the pumping node of the preceding stage; i.e. a forward control scheme is used where the voltage at each pumping node controls the on/off operation of the next stage.

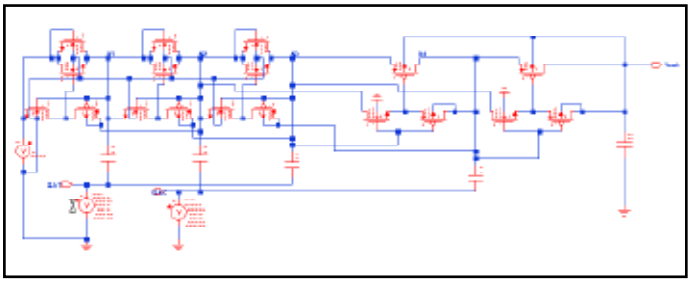


Fig. 12: 4-Stage Schematic of Proposed Charge Pump

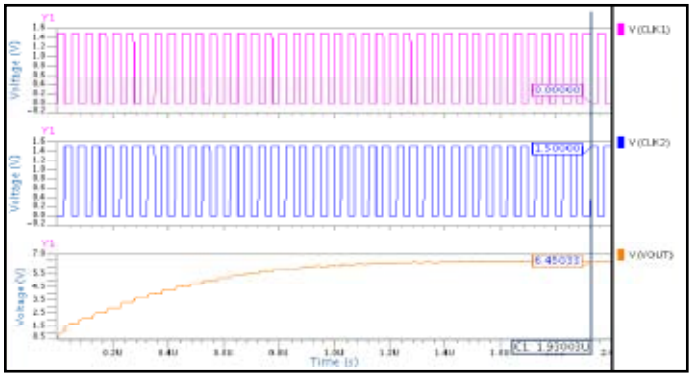


Fig. 13: Output Waveform of 4-Stage Proposed Charge Pump

III. Result

A. Parameters

Dickson	static	Dynamic	High Efficiency	Proposed
1.5	2	2.45	4.3	4.39
2.9	4.3	5.4	5.95	6.42
4.5	5.9	7.3	8.1	8.43
6.2	7.3	9.2	9.7	10.4
8	9.1	11.1	11.9	12.3
9.4	10.7	12.9	13.5	14.1
11.2	12.6	14.8	15.8	16
13.1	14.2	16.7	17.1	17.8
15	16	18	18.9	19.7

1. Pumping Capacitors- 2pf
2. Technology used-180nm
3. Width of NMOS-1.4micron
4. Vin-1.5V
5. Clk Frequency-25MHz

B. Results of Dickson Charge Pump

1. Output Voltage- 3.16080V
2. Power dissipation- 13.2168pW

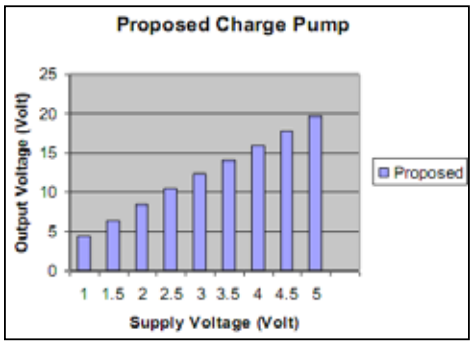
C. Results of Static Charge Pump

1. Output Voltage- 4.4973V
2. Power dissipation- 25.4416pW

D. Results of Dynamic Charge Pump

1. Output Voltage- 5.4621V
2. Power dissipation- 31.3276pW

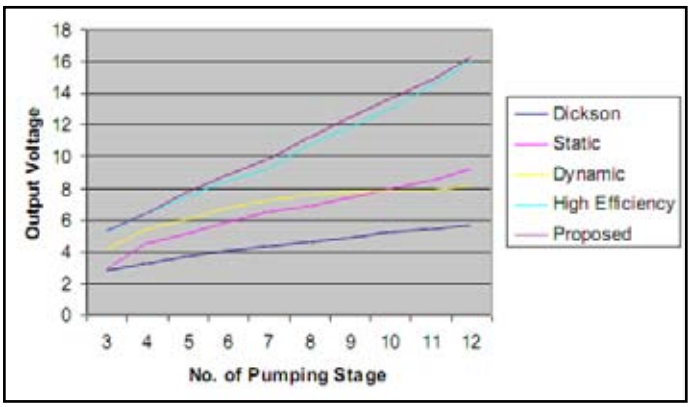
IV. Output Voltage of Proposed Charge Pump With Four Stages Under Different Supply



GRAPH 1: Output voltage of Proposed Charge Pump

No of stages	Output Voltage(V)
3	5.31
4	6.46
5	7.77
6	8.87
7	9.9
8	11.9
9	12.46
10	13.65
11	14.84
12	16.29

Comparison of Different Charge Pump



GRAPH 2: Output voltage of Various Charge Pump

V. Conclusion

A Proposed CMOS charge pump circuit, which uses both the NMOS switches and the PMOS switches to eliminate the body effect, has been designed. A novel CTS control scheme which combines the backward control scheme and the forward control scheme is proposed to obtain high voltage gain. In 180nm CMOS process, the simulation results have shown that much higher pumping efficiency can be achieved by the proposed charge pump compared with other.

VI. References

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