Design of High Speed Ripple Carry Adder Using Mixed Logic Style

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Abstract
This paper presents a circuit design approach to perform very fast carry computation in cascaded full adder. The proposed approach consists of insertion of transmission gate adder between full adders designed by Feedthrough Logic (FTL) approach. A 16-bit ripple carry adder is designed by this proposed approach. Analysis shows that the insertion of transmission-gate full adder between FTL full adders does not violate the timing constraint and perform correct operation. Then a comparison analysis has been carried out by simulating the proposed adder architecture in 0.18 µm technology. The simulation results shows that the proposed adder improves the speed by a factor of 1.157 as compared existing FTL Ripple carry adder.

Keywords
Low Power Feedthrough Logic (LPFTL); Transmission Gate Full Adder (TG-FA); Ripple Carry Adder (RCA)

I. Introduction

In RCA faster carry computation is well known to be a key aspect, since this is the speed limiting factor in case of high speed applications [1]. The RCA consist chain of equal full adders, where carry output of one stage connected to the carry input of next stage as shown in fig. 1. The N^{th} full adder evaluates its carry output $c_{out\ N}$ according the carry output of $(n-1)^{th}$ stage. Hence in cascaded full adder the carry computation limits the overall speed of arithmetic circuits.

The performance of cascaded full adder is related to the carry input-to-carry output delay. Several high speed full adder topologies have been proposed in [1-2]. According to the traditional approach in Fig.1, the same logic style is adopted for all full adders within a RCA.

As compared to the traditional single logic style approach, a mixed logic styles are adopted in a cascaded full adder. In this paper two very fast logic styles i.e. modified low power Feedthrough Logic full adder (LPFTL-FA) and transmission gate full adder (TG-FA) are mixed to achieve very high speed RCA.

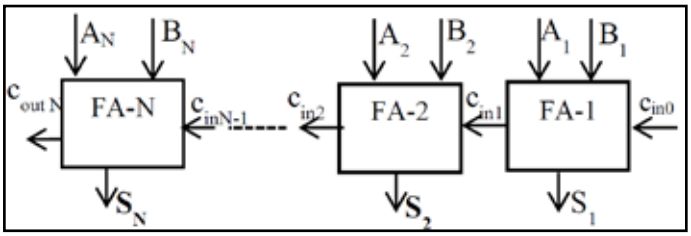

Fig. 1: Chain of N Equal Full Adder

The rest of the sections are organized as follows, section II presents the high speed full adder topologies in single logic style, section III presents the proposed mixed LPFTL/TG full adder, section IV presents the performance analysis of a 16-bit RCA designed by proposed mixed approach and conclusions are derived in section V.

II. Cascaded Full Adder Topologies in Single Logic Style

Full adder consist two logic blocks i.e. sum logic which generates the sum output (s) and carry logic which generates the carry output (C_{out}) according to the inputs. As discussed above, the speed factor is limited by the carry logic which is given by [3-4].

$C_{out} = C_{in}\ (A \oplus B) + AB$

As the carry logic is responsible for high speed RCA design hence only carry logic using single style approach is discussed below,

A. Low Power FTL Full Adder (LPFTL-FA)

The carry logic block for LPFTL-FA [5] is shown in fig. 2. It consists of a NMOS reset transistor (T_n) and pull up PMOS load transistor T_{p1} in series with T_{p2}. T_{p1}, T_{p2} and T_n are controlled by the clock signal (CLK). The basic principle of operation is briefly described here. During CLK =1 (Reset phase), the output node (C_{out}') is pulled to ground through T_n. When CLK goes from 1 to 0 C_{out}' is evaluated depending upon the input A, B, C_{in}. This LPFTL-FA is faster as compared to the other logic style because output node makes partial transition from an intermediate voltage to logic HIGH or LOW as shown in fig. 3. [6-7]. A RCA is designed by cascading this full adder.

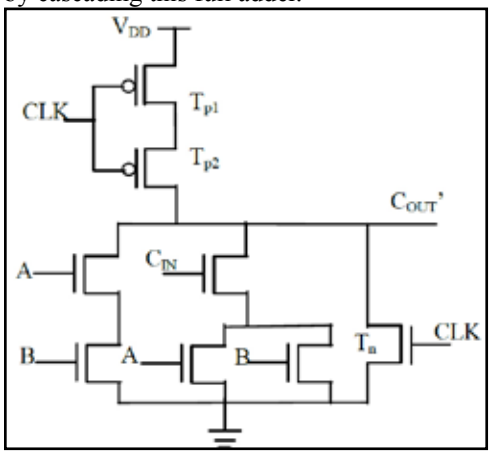

Fig. 2: Carry Logic Using LPFTL

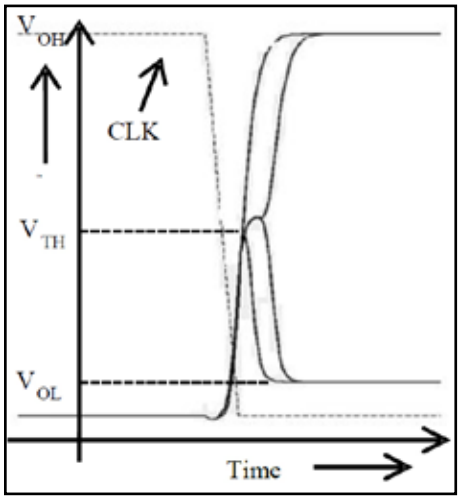

Fig. 3: Output Node Switching Voltage in a Cascaded Structure

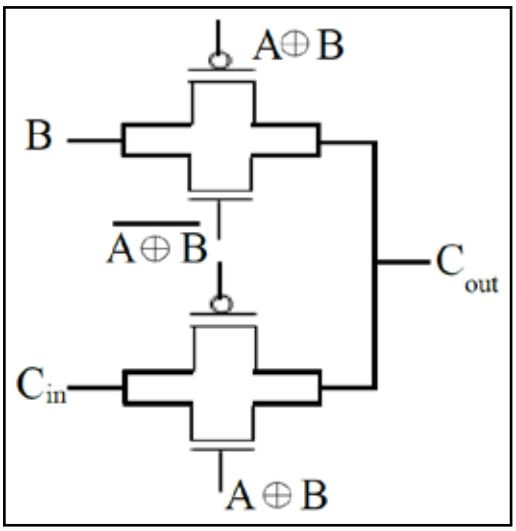

Fig. 4: Carry Logic Using Transmission Gate

B. Transmission Gate Full Adder (TG-FA)

The carry logic for a full adder designed by transmission gate is shown in Fig. 4. Single stage TG-FA is more energy efficient than LPFTL-FA, but performance severely degrades when cascading these FA blocks due to lack of driving capability [8]. For this reason RCA designed by cascading this TG-FA is not suitable for high speed applications.

III. Proposed Mixed FTL/TG RCA

The speed of RCA designed by single style approach depends upon the type of logic style is adopted. The speed of RCA can be improved by mixing two high speed logic styles i.e. by alternating the single style FA chain with two different high speed logic styles as shown in Fig.5. The LPFTL-FA and the TG-FA discussed above are used for this purpose. As shown in Fig.5. TG-FA is used in between LPFTL-FA. The LPFTL-FA increases the overall speed of RCA as well as the proposed mixed style approach is also energy efficient due to low energy consumption of TG-FA. Furthermore, the driving capability of cascaded TG logic style is also improved by the intermediate LPFTL.

During reset phase of LPFTL the carry input of all TG-FA becomes Zero. The carry propagation delay is being measured during the evaluation phase of LPFTL, when valid inputs are applied. Since the intermediate carry are partially evaluated during reset phase, hence overall carry evaluation becomes faster.

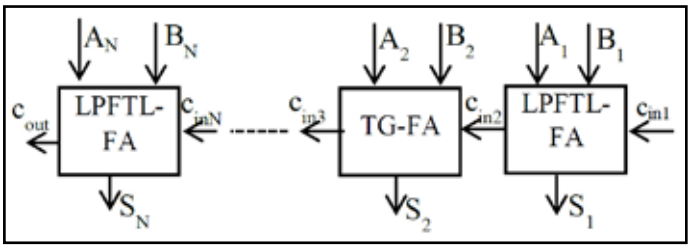

Fig. 5: Mixed LPFTL-FA/TG-FA Chain

IV. Performance Analysis of Mixed FTL/TG RCA

The 16-bit RCA designed by the mixed logic style is simulated at 27 ^{0}C by using 0.18 µm CMOS process technology from UMC. Power supply VDD is constant for all simulation and is equal to 1.8V. Circuits are simulated in HSPICE simulator.

The power and performance comparison at 10fF capacitive load at the output of carry cell at 50MHz clock is shown in Table I. From the simulation result the proposed mixed LPFTL/TG RCA is 1.28 & 1.157 times faster than single style TG-RCA & LPFTL-RCA respectively. The PDP of the proposed structure is also improved.

Table 1. Simulation Results For For 16-Bit Ripple Carry Adder

Logic family	P_{avg} (mW)	t_p (ns)	PDP (mW*nS)
TG in [8]	20.651	7.25	149.719
LPFTL in [5]	25.121	6.512	163.58
Proposed Mixed LPFTL/TG	22.143	5.625	124.55

The variation in average propagation delay with respect to load capacitance is shown in fig. 6. At higher value of load capacitance and temperature the proposed circuit is much faster as compared to LPFTL in [5].

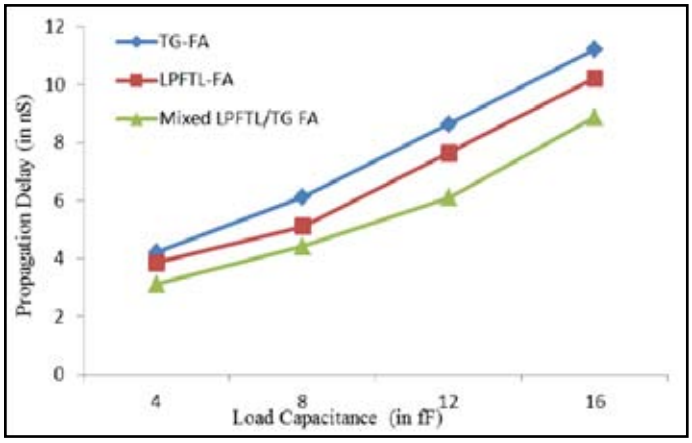

Fig. 6: Effect of Output Load on Propagation Delay

V. Conclusion

In this paper we proposed a mixed LPFTL/TG RCA topologies to achieve a very fast carry computation, as opposite to the traditional approach. The proposed circuit is simulated in 0.18 µm CMOS process technology from UMC. The proposed mixed LPFTL/TG RCA topologies when compared with the traditional single style approach it provide a speed up factor of at-least 1.2. The simulation result confirms that for a given load and at same frequency of operation the power delay product of proposed circuits is much better than that of existing single style approach.

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