Optimization of Total Harmonic Distortion in Multilevel Inverter Using Genetic Algorithm

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Abstract

So far several methods have been presented to optimize the total harmonic distortion in multilevel inverter & maintain the fundamental component at the desired value. This paper focus on elimination of harmonics in a cascaded Hbridge 11 level inverter. The heuristic technique is implemented to find out the minimum THD in cascade multilevel inverter. Using the mathematical theory of resultants, all solutions to this equivalent problem can be found. Theoretical results are verified by simulation and experiments for an 11-level H-bridge inverter. Results show that the proposed method effectively eliminate a great number of specific harmonics, and the output voltage is resulted in low total harmonic distortion.

Keywords

H-bridge Inverter, Harmonics, Genetic Algorithm

I. Introduction

Harmonics must always be limited below threshold level prescribed by standards [1]. Several techniques have been proposed to cancel out high amplitude harmonics to eliminate or reduce the need for filtering while meeting the standard requirements. The most interesting one includes programmed harmonic elimination [2] and multilevel converters, which do not require high frequency switching as the PWM (Pulse Width Modulation) techniques do. Therefore the multilevel converters have attracted much attention in high power application. Among the different topologies for multilevel converters, the cascaded multilevel inverter has received special attention due to its modularity and simplicity of control. The principle of operation of this inverter is usually based on synthesizing the desired output voltage waveform from several steps of voltage, which is typically obtained from dc voltage sources. There are different power circuit topologies for multilevel converters. The most familiar power circuit topology for multilevel converters is based on the cascade connection of an "s" number of single-phase full-bridge inverters to generate a (2s + 1) number of levels. To control the output voltage and to eliminate the undesired harmonics in multilevel converters with equal dc voltages, To control the output voltage and to eliminate the undesired harmonics in multilevel converters with equal dc voltages, various modulation methods such as sinusoidal pulse width modulation (SPWM), space vector PWM techniques are suggested in [3] and [4]. Another approach is to choose the switching angles so that specific higher order harmonics such as the 5th, 7th, 11th, and 13th are suppressed in the output voltage of the inverter. This method is known as Selective Harmonic Elimination (SHE) or programmed PWM techniques in technical literature [5]. Such method is associated with the arithmetic solution of nonlinear transcendental equations which contain trigonometric terms. This set of nonlinear equations can be solved by iterative techniques such as the Newton–Raphson method. However, such techniques need a good initial guess which should be very close to the exact solution patterns. Furthermore, this method finds only one set of solutions depending on the initial guess. Therefore, the Newton–Raphson method is not feasible to solve the SHE problem for a large number of switching angles if good initial guesses are not available. In this paper the total harmonics are reduced by selected harmonics elimination technique in cascade multilevel inverters. In literature there are several techniques are proposed to do so. In this paper GENETIC ALGORITHM technique is proposed to minimize the THD. In this the asymmetry of the transcendental equation set are solved and the simulation results for an 11-level cascaded multilevel inverter are discussed. The paper is organized as follows – cascaded multilevel inverters are discussed in section II. The GA technique is discussed for minimizing the THD is given in section III . The experimental result shown in section IV,V. Section VI & VII followed by conclusion & reference.

II. Cascaded Multilevel Inverter

The cascaded H-bridge multilevel inverter consists of a series of single-phase H-bridge inverter units, as shown in fig. 1. It is modular in nature and can be extended to any required number of levels. It is supplied from several separate dc sources (SDCSs), which may be obtained from batteries, solar cells, or ultra-capacitors Each SDCS is connected to a single-phase H-bridge inverter and can generate three different voltage outputs, +Vdc, 0, and −Vdc. This is accomplished by connecting the dc source to the ac output side by using different combinations of the four switches Q1, Q2, Q3, and Q4. The ac outputs of the modular H-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of all of the individual inverter outputs. All semiconductor devices of the Hbridges are only switching at the fundamental frequency, and consequently this is referred to as the fundamental switching scheme. Also, each H-bridge unit generates a quasi-square waveform by phase-shifting its positive and negative phase legs" switching timings". The number of output voltage levels in a cascaded multilevel inverter is then 2s+1, where s is the number of dc sources. Three-phase version of this circuit is also available by adding another two phases and connecting their neutral point together. Fig. 2 shows the generalized output voltage of cascaded Hbridge multilevel inverter with non-equal dc sources. The total output voltage is given by vo= v1+v2+ v3+......+ vs. With enough levels and an appropriate switching angles θ1, θ2, …. θi , and θs the multilevel inverter results in an output voltage that is almost sinusoidal with a low THD with each of the active devices subjected to a single dc source, and only switching at the fundamental frequency. This reduces both the voltage stress and the switching losses of the semiconductor devices, resulting in a better utilization and high overall efficiency.
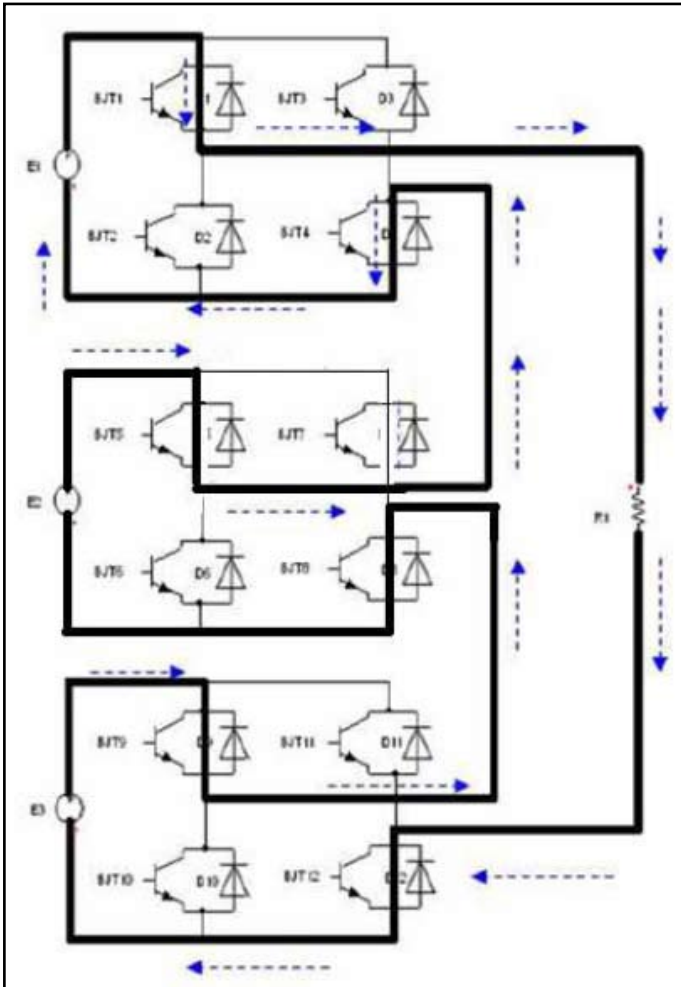
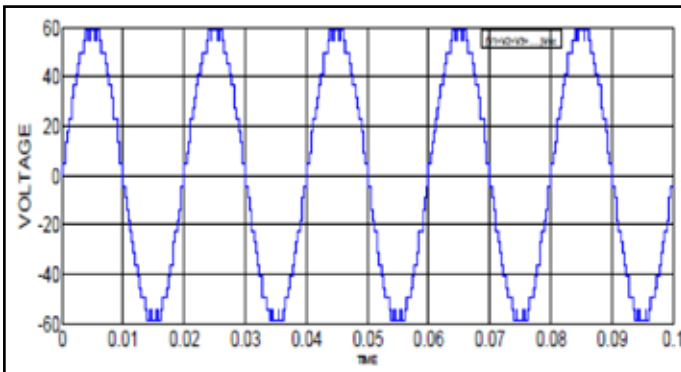Fig. 1: Cascaded H-bridge Multilevel Inverter

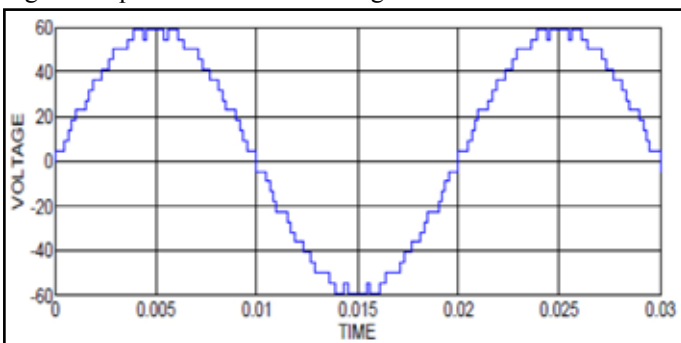Fig. 2: Output of Cascaded H Bridge Multilevel Inverter

Fig. 3: Enlarging of Cascaded Hbridge 11 Level Multi Level Inverter

A. Problem Formulation

Assuming the equal DC source is applied to each of the inverter and taking into consideration the characteristics of the inverter

waveform Fourier series expansion of stepped output voltage waveform of the multilevel inverter with equal dc sources can be expressed as:

$$V_o(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi} [\{\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)\}\sin(\omega t)]$$

Where Vdc is the nominal dc voltage. The above equation has 5 variables ($\theta_1, \theta_2, \theta_3, \theta_4, \theta_5$) where $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \pi/2$. And a set of solutions is obtainable by equating s-1 harmonics to zero and assigning a specific value to the fundamental component, as given below:

Cos (θ_1) + Cos (θ_2) + Cos (θ_3) + Cos (θ_4) + Cos (θ_5) = m
Cos ($3\theta_1$)+ Cos($3\theta_2$)+ Cos($3\theta_3$)+ Cos($3\theta_4$)+ Cos($3\theta_5$) =0
Cos ($5\theta_1$)+ Cos($5\theta_2$)+ Cos($5\theta_3$)+ Cos($5\theta_4$)+ Cos($5\theta_5$) =0
…
…
…
Cos ($n\theta_1$)+ Cos($n\theta_2$)+ Cos($n\theta_3$)+ Cos($n\theta_4$)+ Cos($n\theta_5$) =0

Where, m

$$\frac{V_1}{4Vdc/\pi}$$

is the modulation index. For 11 level inverter where s=5, 3rd, 5th, 7th, 9th order harmonics will be eliminated if single phase Supply is given. In 3 phase case triple harmonics are eliminated automatically. An objective function is then needed for the optimization procedure. In this paper the objective Function which is to be minimized is the total harmonics distortion (THD). The objective function is given by:

$$V1/_{4Vdc/\pi}$$

Where V_1 is the fundamental voltage and V_n is the nth order harmonics voltage.

III. Genetic Algorithm

Genetic algorithm is a directed search algorithms based on the mechanics of biological evolution. It was developed by John Holland, University of Michigan in 1970.It is based on "Darwin"s Theory of Evolution" In the computer science field of artificial intelligence, a genetic algorithm (GA) is a search heuristic that mimics the process of natural evolution. This heuristic is routinely used to generate useful solutions to optimization and search problems. Genetic algorithms belong to the larger class of evolutionary algorithms (EA), which generate solutions to optimization problems using techniques inspired by natural evolution, such as inheritance, mutation, selection, and crossover.

A. Genetic Algorithm for minimizing the THD

1. Randomly initialize the chromosome size and then initialize the iteration size.
2. Find out the objective value (THD) & convert the decimal no. to binary number.
3. Now cross-over between different sets of population.
4. Those chromosomes that are less fittest remove that set of chromosome and initialize new chromosome on that place
5. If maximum iteration reached then terminate or go back to step 3.

IV. Experimental Result

We are using the genetic algorithm in our Matlab Programming in order to obtain the best best firing angle for minimum THD. THD result of the output line voltage up to 49th harmonics was calculated. for this case the THD result was 6.83%. 10 volts dc supply was given to the inverters. The switching angle at which this result has come is as follows $\theta_1 = 1$, $\theta_2 = 2$, $\theta_3 = 5$, $\theta_4 = 6$, $\theta_5 = 16$.in degree. The Fourier transform(FFT) analysis has done and the figure shown below:
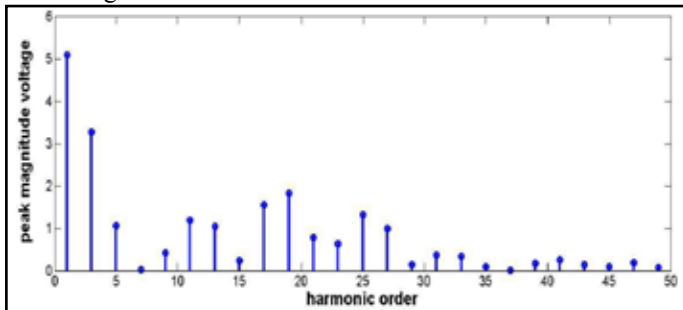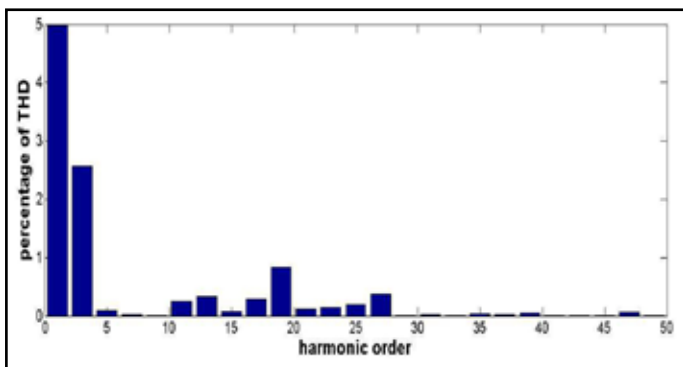

Fig. 4: FFT Analysis for Modulation Index 0.8

Fig. 5: FFT Analysis with Percentage of THD
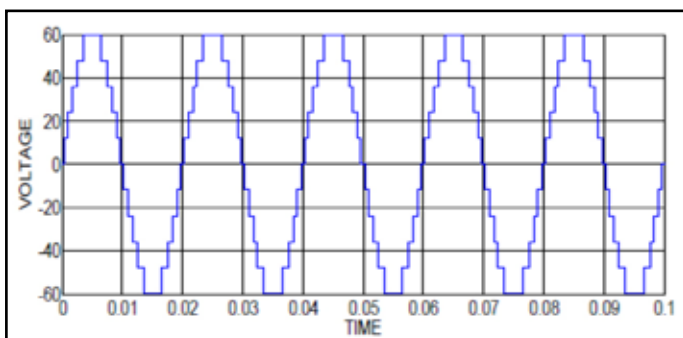
V. Simulation Result

Fig. 6: Output Voltage Wave Form of 11 Level Inverter by Using GA

VI. Conclusion

The prime objective of this project is to develop program on a heuristic technique to minimize the total harmonic distortion with equal D.C sources in H-bridge cascade multilevel inverter. The GA technique presented in this paper achieve this objective and includes:

1. Development of algorithm for minimization of THD.
2. Application of this algorithm in multilevel inverters with equal dc sources which are used in power system to convert the dc power to ac power.
3. Development of simulation to validate the result. This concludes that when the resultant approach reaches the limitation of contemporary algebra software tools, the

proposed methods are able to find the optimum switching angles in a simple manner. We found that by developing logics for the problem, the optimum solution is found out. This method is used less equations,

Less derivations and took less time than that of the other methods of harmonic elimination discussed in chapter to solve the problem. The convergence criteria are very smooth. The simulation and experimental results are provided for an 11-level cascaded H-bridge inverter to validate the accuracy of the computational results. From the experiment we found that the percentage of THD is minimized in GA technique.

References

[1] IEEE recommended practices and requirements for harmonic control in electrical power system IEEE standard, 1992.
[2] M. Sarvi, M. R. Salimian, "Optimization of Specific Harmonics in Multilevel Converters by GA & PSO", UPEC2010 31st Aug - 3rd Sept 2010 Optimization" IEEE transactions on industrial electronics, Vol. 57, No. 11, 2010.
[3] D. G. Holmes, T. A. Lipo, "Pulse Width Modulation for Power Converters". Piscataway, NJ: IEEE Press, 2003
[4] S. Kouro, J. Rebolledo, J. Rodriguez, "Reduced switching-frequency modulation algorithm for high Power multilevel inverters", IEEE Trans.Ind. Electron., Vol. 54, No.5, pp. 2894– 2901, Oct. 2007
[5] W. Fei, X. Du, B. Wu, "A generalized half-wave symmetry SHE-PWM formulation for multilevel voltage inverters," IEEE Trans.Ind. Electron., Vol. 57, No. 9, pp. 3030– 3038, Sep. 2010.
[6] Leon M. Tolbert, John N. Chiasson, Zhong Du, Keith J. McKenzie, "Elimination of Harmonics in a Multilevel Converter", IEEE transactions on application industry, Vol. 41, No. 1, January/Februry 2005.
[7] Jagdish Kumar, et all, "Selective Harmonic Elimination Technique for a Multilevel Inverter", Fifteenth National Power Systems Conference (NPSC), IIT Bombay, December 2008.
[8] Burak Ozpineci, Leon M. Tolbert, John N. Chiasson, "Harmonic Optimization of Multilevel Converters Using Genetic Algorithms", 2004 35th Annul IEEE Power Electronics Specialisu Conference.

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