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FPGA Implementation of 4-Bit Multipliers

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Abstract
Multiplication is one of the basic arithmetic operations and fundamental building block in all DSP task. The objective of good multiplier is to provide a physically compact, good speed and low power consumption. To save significant power consumption in VLSI design, it is good to reduce its dynamic power that is major part of total power dissipation. In this paper we present a comparative study of Array Multiplier, Wallace Tree Multiplier, Booth Multiplier for Area, Power, Speed in VLSI design of 4 bit Multipliers.

Keywords
Multiplier, Multiplication, Array Multiplier, Wallace Tree Multiplier, Booth Multiplier, RTL Design

I. Introduction

As the scale of integration keeps growing more and more sophisticated signal processing system are being implemented on a VLSI chip. Theses signal processing application not only demand great computation capacity but also consume considerable amounts of power. While performance and area remains to be two major design goals, power consumption has become a critical concern in today's VLSI system design. Power dissipation is recognized as a critical parameter in modern VLSI design field. Dynamic power dissipation which is a major part of total power dissipation is due to the charging and discharging capacitance in the circuit. The formula for calculation of dynamic power dissipation is Pd = CLV2f [14]. Power reduction can be achieved by various methods. They are reduction of output capacitance CL, reduction of power supply voltage V, reduction of switching activity and clock frequency.

With the constant growth of computer applications such as computer graphics and signal processing, fast arithmetic unit especially multipliers are becoming increasingly important [11]. Many multimedia and DSP applications are highly multiplication intensive so that the performance and power consumption of these systems are dominated by multipliers [8]. Reducing the power consumption for multiplication can be tackled at different level of design hierarchy [6].

Multiplication is a fundamental operation in most signal processing algorithm. Multipliers have large area, long latency and consume considerable power. There has been extensive work on low-power multiplier at technology, physical circuit and logic levels. More ever power consumption is directly related to data switching patterns. Fast multipliers are a key topic in the VLSI design of high speed processors [1] .

In the past, multiplication was implemented using a sequence of addition subtractions and shift operation. Multiplication can be considered as a series of repeated addition. Each step of addition generates a partial products. This repeated addition method that is suggested by the arithmetic definition is slow that is almost always replace by algorithm that makes use of positional representation [14]. This paper addresses high-level optimization techniques for 4-bit multipliers. High-level techniques refer to algorithm and architecture level techniques that consider multiplication's arithmetic features and input data characteristics. Some of the important algorithm presents in paper for VLSI implementable fast multiplication is Booth Multiplier, Array Multiplier and Wallace Tree Multiplier using Xilinx and Cadence tool.

II. Multiplier

A basic multiplier can consist of three parts:

- Partial product generation
- Partial product addition and
- Final addition [12].

A multiplier essentially consist of two operands ,a multiplicand "Y" and a multiplier "X" and produces a product "P". In a conventional multiplier, a number of partial products are formed first by multiplying the multiplicand with each bit of multiplier. These partial product are then added together to generate the Product "P". In short ,we can break down multiplication into two parts ,namely partial product generation and partial product accumulation. Speeding up multiplication therefore must aim

- Speeding up partial product generation (PPG),
- Reduce the number of partial products,
- Speeding up partial product summation or
- A combination of one or more of the above [9].

III. Basic Multiplication Operation

The most basic form of multiplication consists of forming the product of two binary numbers m and n. (m×n) bit multiplication can be viewed as forming n partial product of m bits each, and then summing appropriately shifted partial products to produce an (m+n) bit result P. Binary multiplication is equivalent to a logical AND operation. Let A and B be the operands with m and n bits respectively. Using shift and add type of approach the product P of these two operands can be represented as shown in equation.

$$A=[\sum_{j=0}^{m-1} a_j 2^j] \qquad B=[\sum_{i=0}^{n-1} b_i 2^i]$$

$$P=[\sum_{j=0}^{m-1} a_j 2^j][\sum_{i=0}^{n-1} b_i 2^i]$$

$$=\sum_{j=0}^{m-1}\sum_{i=0}^{n-1} a_j b_i 2^{i+j}$$

A Binary Multiplier is an electronic hardware device used in digital electronics or a computer or other electronic device to perform rapid multiplication of two numbers in binary representation. It is built using binary adders. The rules for binary multiplication can be stated as follows:

- If the multiplier digit is a 1, the multiplicand is simply copied down and represents the product.
- If the multiplier digit is a 0 the product is also 0.

IV. Methods and Performances

There are number of techniques that can be used to perform multiplication. In general, the choice is based upon factors such as latency, throughput, area, and design complexity [7]. Array Multiplier, Booth Multiplier and Wallace Tree Multipliers are some of the standard approaches to have hardware implementation

of binary Multiplier which are suitable for VLSI implementation at CMOS level

A. Array Multiplie

Array Multiplier is an efficient method of a combinational multiplier. Array Multiplier is common in multiplier design due to its regular and compact structure. The structure of Array Multiplier is organized by several stages of adder and AND-gates [2]. It generates all the partial products after only one AND-gate delay. Then, it sums up all partial products sequentially. The advantage of this structure is that the arrangement of its adders is very regular and is favorable for layout due to this advantage [13].

In Array Multiplier, consider two binary numbers A and B, of m and n bits. There are mn summands that are produced in parallel by a set of mn AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n^2 AND gates. Also, in Array Multiplier worst case delay would be (2n+1) t_d [1]

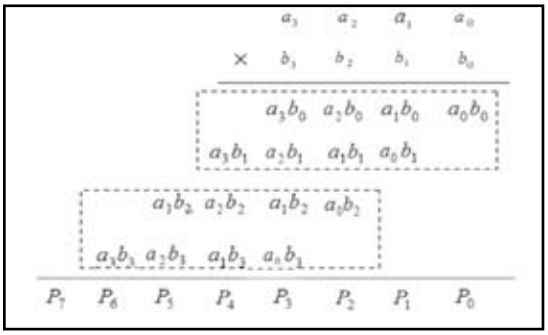

Fig. 1: 4 x4 Basic Multiplication

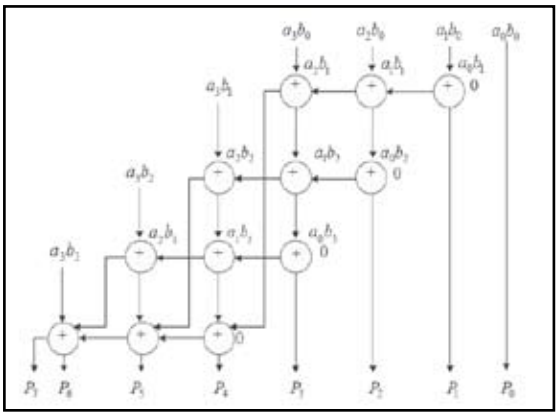

Fig. 2: Ripple Carry Array Multiplier

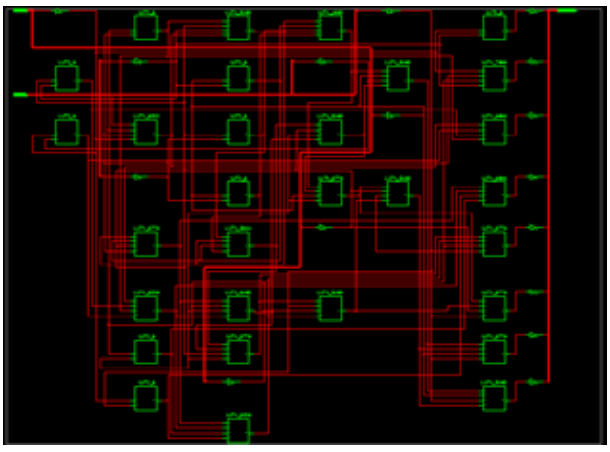

Fig. 3: RTL Schematic of Array Multiplier

Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this Array Multiplier is less economical [4].

B. Wallace Tree Multiplier

A fast process for multiplication of two numbers was developed by Wallace [7]. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product.

In the Wallace Tree method, three bit signals are passed to a one bit full adder ("3W") which is called a three input Wallace Tree circuit, and the output signal (sum signal) is supplied to the next stage full adder of the same bit, and the carry output signal thereof is passed to the next stage full adder of the same no of bit, and the carry output signal thereof is supplied to the next stage of the full adder located at a one bit higher position [5].

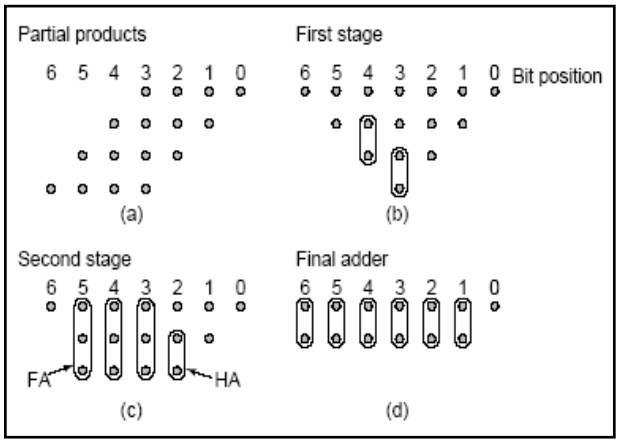

Fig. 4: Logic used in Wallace Tree Multiplier

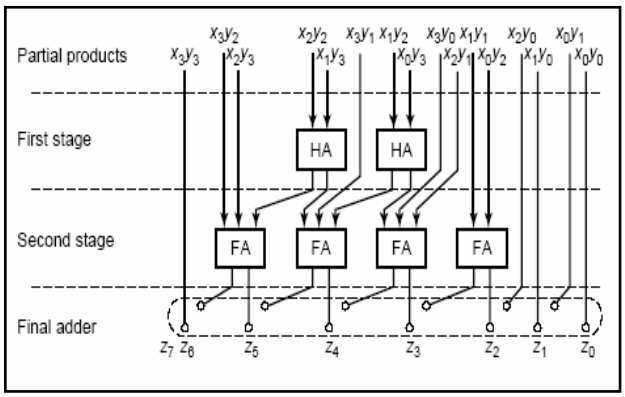

Fig. 5: Wallace Tree Multiplier

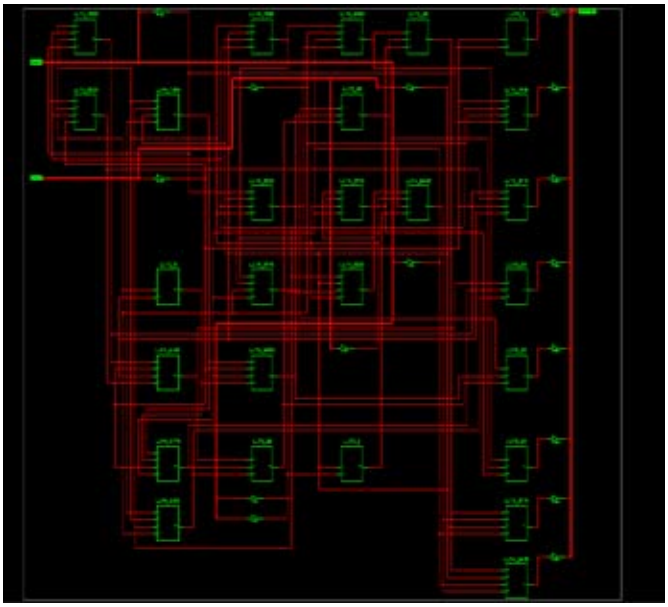

Fig. 6: RTL Schematic of Wallace Tree Multiplier

In the Wallace Tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular. Delay and Power dissipation of Wallace Tree Multiplier is least whereas Array Multiplier is a best for reduced area applications but not speed [3].

C. Booth Multiplier

One improvement in the multiplier is by reducing the number of partial products generated. Booth Algorithm based on the fact that only fewer partial product needs to be generated for a multiplier consisting of consecutive ones or zeros [10]. The Booth Multiplier scans the two bits at a time to reduce the number of partial products.

Table 1: Possible Arithmetic Actions

Bits	Operation Performed
00	no arithmetic operation
01	add multiplicand to left half of product
10	subtract multiplicand from left half of product
11	no arithmetic operation

To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder subtractor is nearly as fast and small as a simple adder.

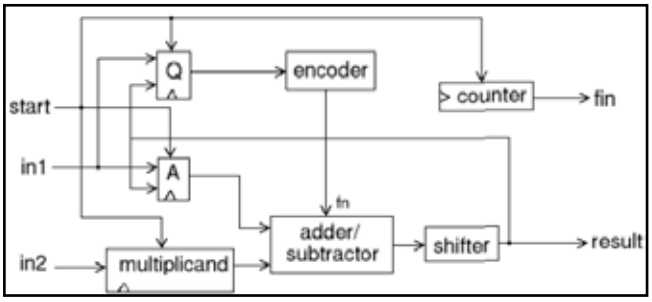

Fig. 7: Booth Multiplier

From the basics of Booth Multiplication it can be proved that the addition/subtraction operation can be skipped if the successive `bits in the multiplicand are same. If 2 consecutive bits are same then addition/subtraction operation can be skipped. Thus in most of the cases the delay associated with Booth Multiplication are smaller than that with Array Multiplier. However the performance of Booth Multiplier for delay is input data dependent. The high performance of Booth Multiplier comes with the drawback of power consumption. The reason for this is the large number of adder cells that consume more power [5].

Fig. 8: RTL Schematic of Booth Multiplier

D. Multiplier Performance and Comparison

The performance comparison of Array Multiplier, Wallace Tree Multiplier, Booth Multiplier are listed in Tables 2 & Table 3, in terms of number of occupied slices, number of 4 input LUT using Xilinx and power, delay using Cadence tool. The simulation results of number of occupied slices and number of 4 input LUT are shown in Table 2. The simulation results of power and delay are shown in Table 3.

Table 2: Simulation Result using Xilinx

Multiplier	Number of 4 input LUTs	Number of occupied Slices
Array Multiplier	30	17
Wallace Tree Multiplier	27	15
Booth Multiplier	26	16

Table 3: Simulation Result using Cadence

Multiplier	Power (uW)		Time Dealy (psec)
	Leakage Power	Dynamic Power	
Array Multiplier	0.936	9.154	1.006
Wallace Tree Multiplier	1.078	10.836	0.921
Booth Multiplier	3.029	15.546	0.862

From these simulation results using Xilinx and Cadence tools, it is evident that the Booth Multiplier requires lesser number of 4 input LUT and time delay than Array Multiplier and Wallace Tree Multiplier.

IV. Conclusions

It can be concluded that Booth Multiplier is superior in respect like speed, delay, area, complexity. However Array Multiplier requires more number of components and large delay than Wallace Tree and Booth Multiplier. But the advantage of Array structure is that the arrangement of its adders is very regular and is favorable for layout. Wallace Tree Multiplier having small area and less delay than Array Multiplier, but due to its higher complexity, its layout is complex. Hence for small area requirement and for less delay requirement Booth's Multiplier is suggested.

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